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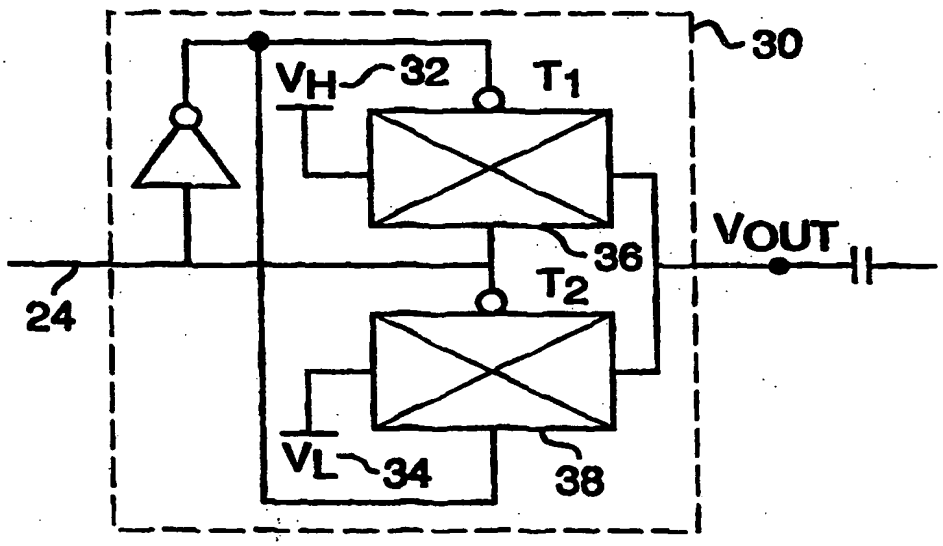
(54) Title: A DRIVER CIRCUIT FOR LOW VOLTAGE OPERATION OF A SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG TO DIGITAL (A/D) CONVERTER AND METHOD THEREFOR

(57) Abstract

A driver circuit for low voltage operation of a Successive Approximation Register (SAR) based Analog/Digital (A/D) converter is disclosed. The driver circuit has a plurality of cells wherein each cell is used for driving an individual column of a capacitor array. A switching circuit is held within each of the plurality of cells. The switching circuit is used for outputting one of a high voltage level V_H or a low voltage level V_L to an individual column of the capacitor array while driving no DC current. The switching circuit is comprised of a pair of fully differential pass gates. The pass gates are driven by circuitry referenced off of the supply voltage V_{dd} of the A/D converter integrated circuit and ground. Because of this, each pass gate may operate off of any voltage within the V_{dd} to ground range. Thus, the switch circuit allows for low voltage operation with a wider operating range. Further, the SAR selects and loads a different bit (112A) of the driver circuit (112) on each edge of a clock cycle. Preferably the converter uses a C-2C network (214'').



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A DRIVER CIRCUIT FOR LOW VOLTAGE OPERATION OF A SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG TO DIGITAL (A/D) CONVERTER AND METHOD THEREFOR

RELATED APPLICATIONS

This application is related to the applications entitled "A SUCCESSIVE APPROXIMATION REGISTER (SAR) FOR CONTROLLING SAMPLING AND CONVERSION OF AN ANALOG TO DIGITAL (A/D) CONVERTER AND METHOD THEREFOR",in the name of Prado et al., and "A CAPACITOR ARRAY FOR A SUCCESSIVE APPROXIMATION REGISTER (SAR) BASED ANALOG TO DIGITAL (A/D) CONVERTER AND METHOD THEREFOR", in the name of the same inventor as the present Application, all filed concurrently herewith, and assigned to the same assignee as this Application. The disclosures of the above referenced applications are hereby incorporated by reference into this application.

BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates generally to Analog to Digital (A/D) converters and, more specifically, to a driver circuit for low voltage operation of a Successive Approximation Register (SAR) based Analog to Digital (A/D) converter and a method therefor.

Description of the Prior Art:

Currently in a Successive Approximation Register (SAR) based A/D converter, an SAR is used to signal a driver circuit to activate different columns of a capacitor array. The driver circuit is presently made up of a plurality of cells wherein each cell is used to drive a respective column of the capacitor array. In its simplest form, each cell houses an inverter which drives its respective column to either V_H or V_L.

The problem with using an inverter is that the lowest voltage the driver circuit may operate at is the lowest operating voltage of the inverter. The lowest operating voltage of an inverter is generally $2V_T$ where V_T is the threshold voltage of the transistors that comprise the inverter. Even at this level, one experiences slow response times.

The A/D converter generally has a digital voltage V_{dd} and a digital ground. In

general, the digital voltage V_{dd} is the operating voltage of the integrated circuit (IC). For analog sampling there is generally a V_H and V_L on which the samples are based. Since the operating voltage of the inverter is $2V_T$, the inverters limit the sampling range V_H to V_L.

Therefore, a need existed to provide an improved driver circuit for an SAR based an A/D converter. The improved driver circuit must be able to operate at lower voltages than a standard inverter circuit. The improved driver circuit must also allow for a wider analog sampling range.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, it is an object of the present invention to provide an improved driver circuit for an SAR based A/D converter.

It is another object of the present invention to provide an improved driver circuit for an SAR based A/D converter that is able to operate at lower voltages than a standard inverter circuit.

It is still another object of the present invention to provide an improved driver circuit for an SAR based A/D converter that has a wider analog sampling range.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENTS

In accordance with one embodiment of the present invention, a driver circuit for low voltage operation of a Successive Approximation Register (SAR) based Analog/Digital (A/D) converter is disclosed. The driver circuit has a plurality of cells wherein each cell is used for driving an individual column of a capacitor array. A switching circuit is held within each of the plurality of cells. The switching circuit is used for outputting one of a high voltage level V_H or a low voltage level V_L to an individual column of the capacitor array while driving no DC current. The switching circuit is comprised of a pair of fully differential pass gates. The pass gates are driven by circuitry referenced off of the supply voltage V_{dd} of the A/D converter integrated circuit and ground. Because of this, each pass gate may operate off of any voltage within the V_{dd} to ground range. Thus, the switching circuit allows for low voltage operation with a wider operating range.

In accordance with another embodiment of the present invention, a method of providing a driver circuit for low voltage operation of a Successive Approximation Register (SAR) based Analog/Digital (A/D) converter is disclosed. The method comprises the steps of providing a plurality of cells wherein each cell is used for driving an individual column of

a capacitor array; and providing a switching circuit within each of the plurality of cells for outputting one of a high voltage level V_H or a low voltage level V_L while driving no DC current. The switching circuit is comprised of a pair of fully differential pass gates. The pass gates are driven by circuitry referenced off of the supply voltage V_{dd} of the A/D converter integrated circuit and ground. Because of this, each pass gate may operate off of any voltage within the V_{dd} to ground range. Thus, the switching circuit allows for low voltage operation with a wider operating range.

The foregoing and other objects, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiments of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified functional block diagram of an Analog to Digital (A/D) converter.

Figure 2 is a simplified functional block diagram of one embodiment of a capacitor array used in the A/D converter depicted in Figure 1.

Figure 3 is a simplified functional block diagram of a second embodiment of a capacitor array used in the A/D converter depicted in Figure 1.

Figure 4 is a simplified functional block of one cell of the driver circuit used in the SAR based A/D converter depicted in Figure 1.

Figure 5 is an electrical schematic of the cell of the driver circuit depicted in Figure 4.

Figure 6 is a simplified functional block diagram of an SAR based Analog to Digital (A/D) converter.

Figure 7 is a simplified functional block diagram of the sampling and conversion circuit of the present invention.

Figure 8 is a timing diagram for the sampling and conversion circuit of the present invention.

Figure 9 is a simplified functional block diagram of the selection circuits used in the sampling and conversion circuit of Figure 7.

Figure 10 is a simplified functional block diagram of an Analog to Digital (A/D) converter.

Figure 11 is a simplified functional block diagram of a prior art capacitor

array used in the A/D converter depicted in Figure 10.

Figure 12 is a simplified functional block diagram of the capacitive ladder of the present invention used in the A/D converter depicted in Figure 10.

Figure 13 is a simplified electrical schematic of part of a capacitive branch of the capacitive ladder depicted in Figure 12.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, an Analog to Digital (A/D) converter 10 is shown. The A/D converter 10 has a driver circuit 12 which is used for driving each row of a capacitor array 14. The driver circuit 12 is comprised of a plurality of cells 12A. Each cell 12A is used to drive a specific column or bank of the capacitor array 14. By activating and deactivating each bank within the capacitor array 14, the driver circuit 12 may control the output voltage V_{out} of the capacitor array 14.

The capacitor array 14 may take on several different embodiments. The capacitor array 14 may be in the form of a binary weighted capacitor array 14' as depicted in Figure 2. In the binary weighted capacitor array 14', each capacitor bank 14A' has a capacitance value equal to approximately 2^n where n is an integer greater than or equal to 0. The capacitor array 14 may also take the form of a capacitance ladder 14" as depicted in Figure 3.

Referring back to Figure 1, the output voltage V_{out} of the capacitor array 14 is sent to one input of a comparator 16. A second input of the comparator 16 is coupled to an output of a sampling circuit 20. The sampling circuit 20 has an input coupled to an analog input signal 18. The sampling circuit 20 will sample the analog signal at timed intervals and send the sampled signal to the comparator 16. The comparator 16 will then compare the voltage of the sampled signal to that of the output voltage V_{out} of the capacitor array 14.

After comparing the two input voltage levels, the comparator 16 will send a signal to a Successive Approximation Register (SAR) 22 on whether the output voltage V_{out} was higher or lower than the sampled voltage. The SAR 22 will then signal the driver circuit 12 on which rows of the capacitor array 14 need to be activated and/or deactivated.

In operation, the Most Significant Bit (MSB) of the driver circuit 12 is first set high while all the other bits 12A in the driver circuit 12 are set to zero. The comparator 16 will then compare the output voltage V_{out} of the capacitor array 14 to the sampled voltage from the sampling circuit 20. If V_{out} is greater than the sampled voltage level, the

comparator 16 will signal the SAR 22 that the output voltage V_{out} has over shot the sampled voltage. The SAR 22 will then set the MSB of the driver circuit 12 to zero. The entire process is now repeated for the next cell 12A (i.e., MSB-1). If the output voltage V_{out} does not overshoot the sampled voltage signal, then the cell 12A is a valid bit and is set high. The entire process is carried out for every cell 12A. The driver circuit 12 may then generate a digital output based on the settings of the cells 12A.

Referring now to Figure 4, each cell 12A of the driver circuit 12 stores a switching circuit 30. The switching circuit 30 is used for outputting either a high voltage level V_H or a low voltage level V_L. However, unlike prior art switching circuits, the switching circuit 30 will drive each row of the capacitor array 12 to either V_H or V_L while driving no DC current. The switching circuit 30 is comprised of a pair of fully differential pass gates 36 and 38. The pair of pass gates 36 and 38 are driven by circuitry referenced off of the supply voltage V_{dd} of the A/D converter integrated circuit 10 and ground. Because of this, each pass gate (i.e., 36 or 38) may operate off of any voltage within the V_{dd} to ground range. Thus, the difference between V_H and V_L can be as small as 10mv or as high as the supply voltage V_{dd}. The switching circuit 30 of the present invention thereby allows for low voltage operation with a wider operating range.

Each switching circuit 30 has a first voltage source 32 and a second voltage source 34 for supplying the high and low voltage levels respectively which are used for driving the row of the capacitor array 14. The first pass gate 36 is coupled to the first voltage source 32. The first pass gate 36 is used for outputting the high voltage level V_H to the respective row of the capacitor array 14 while driving no DC current. The second pass gate 38 is coupled to the second voltage source 34. The second pass gate 38 is used for outputting the low voltage level V_L to the respective row of the capacitor array 14 while also driving no DC current. Each pass gate 36 and 38 is coupled to the SAR 22 through the bus 24 (Figure 1). The SAR 22 will activate or deactivate the respective pass gates 36 and 38 by sending data over the bus 24 in order to drive each column of the capacitor array 14 to one of V_H or V_L.

Referring to Figure 5, wherein like numerals and symbols represent like elements, one embodiment of the switching circuit 30 is shown. As can be seen from Figure 5, each pass gate 36 and 38 are comprised of a PMOS transistor and an NMOS transistor coupled together in parallel. The first pass gate 36 has a PMOS transistor 40 and an NMOS transistor 42 both having drain, gate, and source terminals. The source terminal of the

PMOS transistor 40 is coupled to the first voltage source 32 and to the drain terminal of the NMOS transistor 42. The gate terminals of the PMOS transistor 40 and the NMOS transistor 42 are coupled to the bus 24. In the embodiment depicted in Figure 5, the gate terminal of the PMOS transistor 40 is coupled to the bus 24 through an inverter 44. The drain terminal of the PMOS transistor 40 and the source terminal of the NMOS transistors 42 are coupled together and to the output terminal V_{out} of the capacitor array 14.

Likewise, the second pass gate 38 has a PMOS transistor 46 and an NMOS transistor 48 which are coupled together in parallel. Both the PMOS and the NMOS transistors 46 and 48 have drain, gate, and source terminals. The source terminal of the PMOS transistor 46 is coupled to the second voltage source 34 and to the drain terminal of the NMOS transistor 48. The gate terminals of the PMOS transistor 46 and the NMOS transistor 48 are coupled to the bus 24. In the embodiment depicted in Figure 5, the gate terminal of the NMOS transistor 40 is coupled to the bus 24 through the inverter 44. The drain terminal of the PMOS transistor 46 and the source terminal of the NMOS transistors 46 are coupled together and to the output terminal V_{out} of the capacitor array 14.

In operation, the SAR 22 will send a signal through the bus 24 to the respective cells 12A of the driver circuit 12. The signal will activate or deactivate both the first and second pass gates 36 and 38 of the respective switching circuit 30. In the embodiment depicted in Figure 5, if the signal on the bus 24 is a digital high, the PMOS and NMOS transistors 40 and 42 of the first pass gate 36 are activated and the PMOS and NMOS transistors 46 and 48 of the second pass gate 36 are deactivated. Thus, the cell 14A will output a high voltage level output V_H which is used to drive the column of the capacitor array 14. If the signal on the bus 24 is a digital low, the PMOS and NMOS transistors 40 and 42 of the first pass gate 36 are deactivated and the PMOS and NMOS transistors 46 and 48 of the second pass gate 36 are activated. Thus, the cell 14A will output a low voltage level output V_L

The first and the second pass gates 36 and 38 will operate at much lower levels than prior art inverters. This is due to the fact that the pair of pass gates 36 and 38 are driven by circuitry referenced off of the supply voltage V_{dd} of the A/D converter integrated circuit 10 and ground and thus may operate off of any voltage within the V_{dd} to ground range. Since each column of the capacitor array 14 may be switched and driven between a V_L and a V_H from zero to the operating voltage V_{dd}, the present invention allows for a wider range of operation.

Referring to Figure 6, an Analog to Digital (A/D) converter 110 is shown. The A/D converter 110 uses a driver circuit 112 for driving each column of a capacitor array 114. The driver circuit 112 is comprised of a plurality of cells 112A. Each cell 112A is used to drive a specific column or bank of the capacitor array 114. By activating and deactivating each bank within the capacitor array 114, the driver circuit 112 may control the output voltage V_{out} of the capacitor array 114.

The output voltage V_{out} of the capacitor array 114 is sent to one input of a comparator 116. A second input of the comparator 116 is coupled to an output of a sampling circuit 120. The sampling circuit 120 has an input coupled to an analog input signal 118. The sampling circuit 120 will sample the analog signal at timed intervals and send the sampled signal to the comparator 116. The comparator 116 will then compare the voltage of the sampled signal to that of the output voltage V_{out} of the capacitor array 114.

After comparing the two input voltage levels, the comparator 116 will send a signal to a Successive Approximation Register 122 on whether the output voltage V_{out} was higher or lower than the sampled voltage. The SAR 122 will then latch in the proper value for each bit 112A via bus 124.

In operation, the Most Significant Bit (MSB) of the driver circuit 112 is first set high while all the other bits 112A in the driver circuit 112 are set to zero. The comparator 116 will then compare the output voltage V_{out} of the capacitor array 114 to the sampled voltage from the sampling circuit 120. If V_{out} is greater than the sampled voltage level, the comparator 116 will signal the SAR 122 that the output voltage V_{out} has over shot the sampled voltage. The SAR 122 will then latch in a zero to the MSB via the bus 124. The entire process is now repeated for the next cell 112A (i.e., MSB-1). If the output voltage V_{out} does not overshoot the sampled voltage signal, then the cell 112A is a valid bit and is set high. The entire process is carried out for every cell 112A. The driver circuit 112 may then generate a digital output based on the settings of the cells 112A.

Referring to Figure 7, wherein like numerals and symbols represent like elements with the exception of the use of a "'" to indicate a different embodiment, an improved SAR circuit 122' (hereinafter SAR 122') is shown. The SAR 122' is used for selecting and loading a proper value in each bit of the driver circuit 112 (Figure 6) in order to activate and deactivate the different columns of the capacitor array 114 (Figure 6). The SAR 122' is unique in that the SAR 122' will select and load a different bit 112A (Figure 6) of the driver circuit 112 on each edge of a clock cycle.

The SAR 122' is comprised of a first set of selecting circuits 130. The number of selecting circuits 130 is equal to the total number of odd bits in the driver circuit 112. Each of the selecting circuits 130 is individually coupled to a separate one of the odd number bits of the driver circuit 112. The selecting circuit 130 is used for selecting one of the odd number bits and for latching in a value to the selected odd number bit on a first edge of the clock cycle. The latched in value will drive the select column of the capacitor array 114. Each odd number bit is selected and loaded once during each conversion and is selected and loaded only on a first edge of the clock cycle.

The SAR 122' is further comprised of a second set of selecting circuits 132. The number of selecting circuits 132 is equal to the total number of even bits in the driver circuit 112. Each of the selecting circuits 132 is individually coupled to a separate one of the even number bits of the driver circuit 112. The selecting circuit 132 is used for selecting one of the even number bits and for latching in a value to the selected even number bit on a second edge of the clock cycle. The latched in value will drive the select column of the capacitor array 114. Each even number bit is selected and loaded once during each conversion and is only selected and loaded on a second edge of the clock cycle.

Each of the selecting circuits 130 and 132 are coupled to a clock generator 134. The clock generator is used to provide the clock signal to each of the selecting circuits 132 and 134. In the preferred embodiment of the present invention, two non-overlapping clocks are used for the clock generator.

Referring now to Figures 6-8, a state machine 136 is coupled to the SAR 122'. The state machine 136 is used to generate and send out a plurality of signals prior to each conversion by the A/D converter 110. When the state machine 136 receives a Start of Conversion (SOC) signal (i.e., SOC goes high), the state machine 136 will send a reset pulse to the SAR 122' via bus 124'. The reset pulse will reset and initialize the capacitor array 114 to zero volts. When the reset pulse goes low, the state machine 136 will send out sample and switch signals in order to sample the analog input signal. After the analog input signal has been sampled, the state machine 136 will send out an SAR enable signal to the SAR 122'. The SAR enable signal will cause the SAR 122' to load an initial value into the driver circuit 112.

After the initial value is loaded into the driver circuit 112, on a first edge of a clock cycle, the SAR 122' will cause the Most Significant Bit (MSB) of the driver circuit 112 to be set high while all the other bits 112A in the driver circuit 112 are set to zero. The

comparator 116' will then compare the output voltage V_{out} of the capacitor array 114 to the sampled analog input voltage. If V_{out} is greater than the sampled analog input voltage, the comparator 116' will signal the SAR 122' that the output voltage V_{out} has over shot the sampled voltage. The SAR 122' will then latch in a zero to the MSB via the bus 124'. The entire process is now repeated for the next cell 112A (i.e., MSB-1) on the second edge of the clock cycle. If the output voltage V_{out} does not overshoot the sampled voltage signal, then the cell 112A is a valid bit and is set high. The entire process is carried out for every cell 112A wherein a successive cell 112A will be selected and driven high on the next edge of the clock signal. The driver circuit 112 may then generate a digital output based on the settings of the cells 112A.

Referring to Figure 9, each of the selecting circuits 130 is basically comprised of two latches 140 and 142. The first latch 140 is coupled to the clock generator 134. The first latches 140 are used to select which odd number bit of the driver circuit 112 is to be selected. A single and different odd number bit will be selected on each first edge of the clock cycle. A second latch 142 is coupled to an output of the first latch 140 and to a separate one of the odd number bits of the driver circuit 112. The second latch 142 will load and latch in a proper value to the specific odd number bit in order to drive the particular column of the capacitor array 114 coupled to the selected bit. The first latch 140 sends a signal to the second latch 142. This signal is gated with the signal from the clock generator 134 and with the output from a directly successive latch from an even number bit of the driver circuit 112. When all of the input signals to the logic gate 144 are correct, the second latch 142 will load and latch in the proper value to the selected odd number bit in order to drive the capacitor array 114.

Similar to the selecting circuits 130, each of the selecting circuits 132 are basically comprised of two latches 146 and 148. The first latch 146 is coupled to the clock generator 134. The first latches 146 are used to select which even number bit of the driver circuit 112 is to be selected. A single and different even number bit will be selected on each second edge of the clock cycle. A second latch 148 is coupled to an output of the first latch 146 and to a separate one of the even number bits of the driver circuit 112. The second latch 148 will load and latch in a proper value to the specific even number bit in order to drive the particular column of the capacitor array 114 coupled to the selected bit. The first latch 146 sends a signal to the second latch 148. This signal is gated with the signal from the clock generator 134 and with the output from a directly successive latch from an odd number bit of

the driver circuit 112. When all of the input signals to the logic gate 150 are correct, the second latch 148 will load and latch in the proper value to the selected even number bit in order to drive the capacitor array.

An end of conversion latch 156 is coupled to the last selecting circuit 130 or 132. The end of conversion latch 156 is used for sending an end of conversion signal after the least significant bit of the driver circuit 112' has been loaded with a proper value after the least significant bit has driven its corresponding row of the capacitor array 114.

A reset and enable circuit 152 is coupled to each of the first set of signalling circuits 130 and to each of the second set of signalling circuits 132. The reset and enable circuit 152 is used for resetting and loading an initial value into each of the even and odd number of bits of the driver circuit 112 prior to each conversion. The reset and enable circuit 152 resets and loads each bit via the bus 124'.

Referring to Figure 10, an Analog to Digital (A/D) converter 210 is shown. The A/D converter 210 uses a driver circuit 212 for driving each column of a capacitor array 214. The driver circuit 212 is comprised of a plurality of cells 212A. Each cell 212A is used to drive a specific column or bank of the capacitor array 214. By activating and deactivating each bank within the capacitor array 214, the driver circuit 212 may control the output voltage V_{out} of the capacitor array 214.

The output voltage V_{out} of the capacitor array 214 is sent to one input of a comparator 216. A second input of the comparator 216 is coupled to an output of a sampling circuit 220. The sampling circuit 220 has an input coupled to an analog input signal 218. The sampling circuit 220 will sample the analog input signal 218 at timed intervals and send the sampled signal to the comparator 216. The comparator 216 will then compare the voltage of the sampled signal to that of the output voltage V_{out} of the capacitor array 214.

After comparing the two input voltage levels, the comparator 216 will send a signal to a Successive Approximation Register (SAR) 222 on whether the output voltage V_{out} was higher or lower than the sampled voltage. The SAR 222 will then signal the driver circuit 212 over bus 224 on which rows of the capacitor array 214 need to be activated and/or deactivated.

In operation, the Most Significant Bit (MSB) of the driver circuit 212 is first set high while all the other bits 212A in the driver circuit 212 are set to zero. The comparator 216 will then compare the output voltage V_{out} of the capacitor array 214 to the sampled voltage from the sampling circuit 220. If V_{out} is greater than the sampled voltage level, the

comparator 216 will signal the SAR 222 that the output voltage V_{out} has over shot the sampled voltage. The SAR 222 will then send a signal via bus 224 to the driver circuit 212 to set the MSB to zero. The entire process is now repeated for the next cell 212A (i.e., MSB-1). If the output voltage V_{out} does not overshoot the sampled voltage signal, then the cell 212A is a valid bit and is set high. The entire process is carried out for every cell 212A. The driver circuit 212 may then generate a digital output based on the settings of the cells 212A.

Referring to Figure 11, wherein like numerals and symbols represent like elements with the exception of the use of a "'" to indicate a different embodiment, a prior art capacitor array 214' is shown. The capacitor array 214' depicted in Figure 11 is a binary weighted capacitor array 214'. In the binary weighted capacitor array 214', each capacitor bank 214A' has a capacitance value equal to approximately 2^n where n is an integer greater than or equal to 0. Each capacitor bank 214A' is generally comprised of a plurality of unit capacitors C coupled together in parallel to achieve the capacitor bank's desired capacitive value.

The problem with the binary weighted capacitor array 214' is that for higher bits of resolution, a large number of unit capacitors C are required. For example, for 8 bits of resolution, 256 unit capacitors C are needed, for 10 bits of resolution 1024 unit capacitors C are required, and for 16 bits of resolution 65,536 unit capacitors C are required. Thus, for larger bits of resolution, the binary weighted capacitor array 214' creates a routing nightmare. Furthermore, the binary weighted capacitor array 214' may have parasitic problems since the binary weighted capacitor array 214' will need to drive a large number (2^nC) of unit capacitors.

Referring now to Figure 12 were like numerals and symbols represent like elements with the exception of the use of a "'" to indicate a different embodiment, an improved capacitor array 214" is shown. The capacitor array 214" is a capacitive ladder 214". The capacitive ladder 214" is comprised of a plurality of capacitive branches 214A". Each of the capacitive branches 214A" (with the exception of the last capacitive branch 214B" which is coupled to the LSB) is comprised of a capacitor 226 having a unit capacitance value of C. The capacitor 226 has a first terminal which is coupled to a bit 212A (Figure 10) in the driver circuit 212 (Figure 10). The second terminal of the capacitor 226 is coupled to a capacitor circuit 228 having a capacitance value of 2C. In order to avoid fringing capacitance and matching problems, each capacitor in the capacitive ladder 214" should have a constant perimeter to area ratio. Thus, the capacitor circuit 228 is comprised of two

capacitors 226 coupled together in parallel wherein each capacitor 226 has a unit capacitance value of C (Figure 13).

The last capacitive branch 214B" is also comprised of a capacitor 226 having a unit capacitance value of C. The capacitor 226 has a first terminal which is coupled to the LSB 212A (Figure 10) of the driver circuit 212 (Figure 10). The second terminal of the capacitor 226 is coupled to the first terminal of a second capacitor 230. The second terminal of the second capacitor 230 is coupled to ground. The second capacitor 230 has a capacitance value of C.

In the embodiment depicted in Figure 12, an NMOS transistor 232 is coupled to each of the nodes n_0, n_1, n_2, and n_3. The NMOS transistor 232 is used to drive each of the nodes (n_0, n_1, n_2, and n_3) to a known voltage level prior to each conversion. In the embodiment depicted in Figure 12, the NMOS transistors 232 are used to drive each of the nodes (n_0, n_1, n_2, and n_3) to ground. However, it should be noted that other devices may be used to drive each the nodes (n_0, n_1, n_2, and n_3) to a predetermined value and that the NMOS transistor 232 is just one of many such devices.

The NMOS transistors 232 may cause a parasitic leakage problem. Parasitic leakage will effect the capacitive ladder 214" at high temperatures. Generally, parasitic leakage will affect the output node (V_{out}) the most. As one moves down the capacitive ladder 214", the leakage goes down exponentially (approximately $1/2^n$) and does not affect the output.

For a four bit capacitive ladder 214" (MSB, MSB-1, LSB+1, and LSB), if the MSB is high, the output voltage V_{out} will be 1/2 V_{Full} where V_{Full} is the full scale value of the output voltage V_{out}. If the MSB-1 bit is held high, V_{out} will be 1/4 V_{Full}. If the LSB+1 bit is held high, V_{out} will be 1/8 V_{Full}. If the LSB bit is held high, V_{out} will be 1/16 V_{Full}. Thus, the capacitive ladder 214" will generate a binary weighted output voltage while using considerably less capacitors than the prior art binary weighted capacitor array 214' (Figure 11). By using the capacitive ladder 214", the number of unit capacitors C increases linearly with increasing bits of resolution. In contrast, for a binary weighted capacitor array 214' (Figure 11), the number of unit capacitors C goes up exponentially when the bits of resolution increases. For the capacitive ladder 214", the number of unit capacitors is approximately equal to 3n-1 where n is the total number of the bits of resolution. For the prior art binary weighted capacitor array 214', the number of unit capacitors is approximately equal to 2^n where n is the total number of the bits of resolution. Thus, for 10 bits of

resolution, the capacitive ladder 214" of the present invention will require only 29 unit capacitors C, while the prior art binary weighted capacitor array 214' will require 1024. For 14 bits of resolution, the capacitive ladder 214" of the present invention will only require 41 unit capacitors C, while the prior art binary weighted capacitor array 214' will require 16,384.

By selecting each capacitive branch 214A" to be a C, 2C combination, each branch of the capacitive ladder 214" has the same equivalent capacitance, 2C. Likewise, the last capacitive branch 214B" also has an equivalent capacitance of 2C (capacitors 226 and 230 both having a capacitance value of C coupled together in parallel). Thus, each capacitive branch 214A" and 214B" will be the same size and will switch at the same speed. This will increase the overall speed of the SAR based A/D converter. In contrast, in prior art SAR based A/D converters using a binary weighted capacitor array 214', for 10 bits of resolution, it would be difficult and slow to drive 1024 unit capacitors. Furthermore, a lot of spike current would be generated by driving 1024 unit capacitors.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form, and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A driver circuit for low voltage operation of a Successive Approximation Register (SAR) based Analog/Digital (A/D) converter comprising, in combination:

a plurality of cells wherein each cell is used for driving an individual column of a capacitor array; and

a switching circuit within each of said plurality of cells for outputting one of a first voltage level or a second voltage level while driving no DC current.

2. A driver circuit for low voltage operation of an SAR based A/D converter in accordance with Claim 1 wherein a level of said second voltage level may be as low as ground potential.

3. A driver circuit for low voltage operation of an SAR based A/D converter in accordance with Claim 1 wherein a level of said first voltage level may be as high as a supply voltage of said A/D converter.

4. A driver circuit for low voltage operation of an SAR based A/D converter in accordance with Claim 1 wherein each switching circuit comprises:

a first voltage source for supplying said first voltage level;

a second voltage source for supplying said second voltage level;

a first pass gate coupled to said first voltage source for outputting said first voltage level while driving no DC current;

a second pass gate coupled to said second voltage source for outputting said second voltage level while driving no DC current; and

a signal circuit coupled to said first pass gate and to said second pass gate for activating and deactivating said first pass gate and said second pass gate for outputting one of said first voltage level or said second voltage level.

5. A driver circuit for low voltage operation of an SAR based A/D converter in accordance with Claim 4 wherein each of said first pass gate and said second pass gate comprises:

an NMOS transistor; and

a PMOS transistor coupled in parallel with said NMOS transistor.

6. A driver circuit for low voltage operation of an SAR based A/D converter in accordance with Claim 4 wherein said signal circuit comprises an inverter coupled to a signal bus wherein said signal bus sends data to activate and deactivate each of said plurality of cells of said driver circuit.

7. A driver circuit for low voltage operation of an SAR based A/D converter comprising, in combination:

a plurality of cells wherein each cell is used for driving an individual column of a capacitor array; and

a switching circuit within each of said plurality of cells for outputting one of a first voltage level or a second voltage level while driving no DC current, wherein a level of said second voltage level may be as low as ground potential and a level of said first voltage level may be as high as a supply voltage of said A/D converter, each of said switching circuit further comprising:

a first voltage source for supplying said first voltage level;

a second voltage source for supplying said second voltage level;

a first pass gate coupled to said first voltage source for outputting said first voltage level while driving no DC current;

a second pass gate coupled to said second voltage source for outputting said second voltage level while driving no DC current; and

a signal circuit coupled to said first pass gate and to said second pass gate for activating and deactivating said first pass gate and said second pass gate for outputting one of said first voltage level or said second voltage level.

8. A driver circuit for low voltage operation of an SAR based A/D converter in accordance with Claim 7 wherein each of said first pass gate and said second pass gate comprises:

an NMOS transistor; and

a PMOS transistor coupled in parallel with said NMOS transistor.

9. A driver circuit for low voltage operation of an SAR based A/D

converter in accordance with Claim 7 wherein said signal circuit comprises an inverter coupled to a signal bus wherein said signal bus sends data to activate and deactivate each of said plurality of cells of said driver circuit.

10. A method of providing a driver circuit for low voltage operation of an SAR based A/D converter comprising the steps of:

providing a plurality of cells wherein each cell is used for driving an individual column of a capacitor array; and

providing a switching circuit within each of said plurality of cells for outputting one of a first voltage level or a second voltage level while driving no DC current.

11. The method of Claim 10 wherein a level of said second voltage level may be as low as ground potential.

12. The method of Claim 10 wherein a level of said first voltage level may be as high as a supply voltage of said A/D converter.

13. The method of Claim 10 wherein said step of providing a switching circuit further comprises the steps for each switching circuit of:

providing a first voltage source for supplying said first voltage level;

providing a second voltage source for supplying said second voltage level;

providing a first pass gate coupled to said first voltage source for outputting said first voltage level while driving no DC current;

providing a second pass gate coupled to said second voltage source for outputting said second voltage level while driving no DC current; and

providing a signal circuit coupled to said first pass gate and to said second pass gate for activating and deactivating said first pass gate and said second pass gate for outputting one of said first voltage level or said second voltage level.

14. The method of Claim 13 wherein said steps of providing said first pass gate further comprises the steps of:

providing an NMOS transistor; and

providing a PMOS transistor coupled in parallel with said NMOS transistor.

15. The method of Claim 13 wherein said steps of providing said second pass gate further comprises the steps of:

providing an NMOS transistor; and

providing a PMOS transistor coupled in parallel with said NMOS transistor.

16. The method of Claim 13 wherein said step of providing a signal circuit further comprises the step of providing an inverter coupled to a signal bus wherein said signal bus sends data to activate and deactivate each of said plurality of cells of said driver circuit.

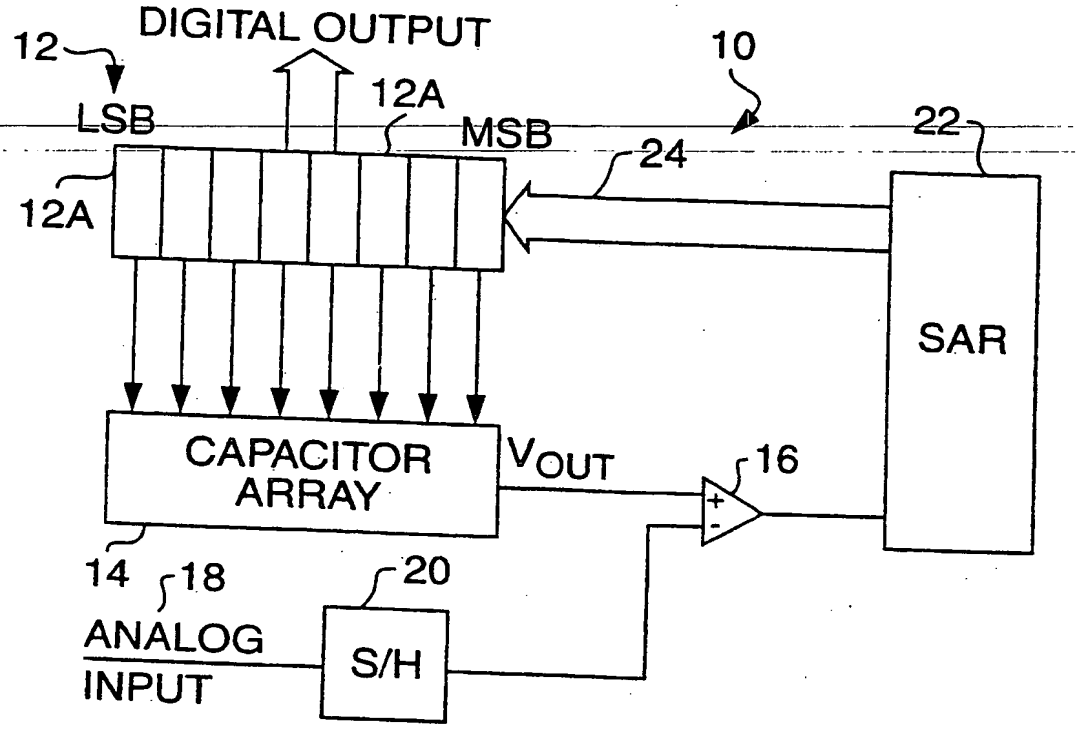

Figure 1

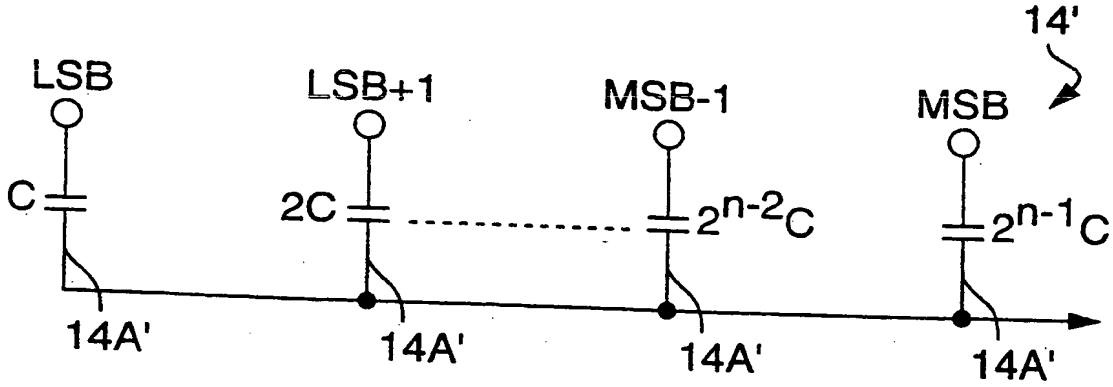

Figure 2

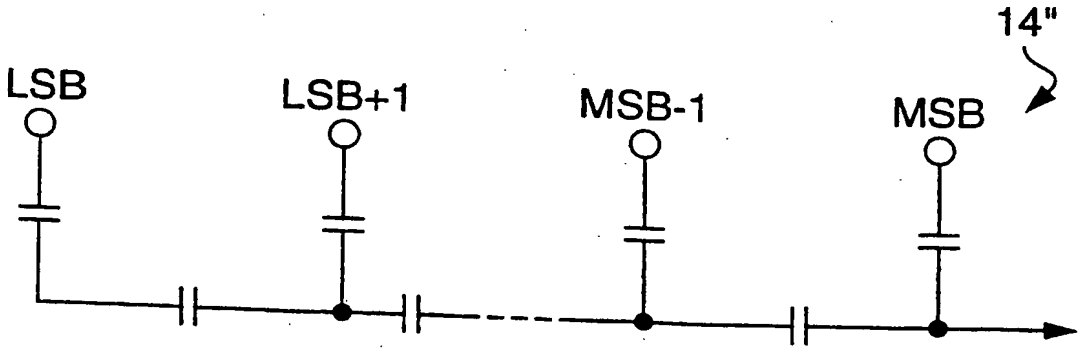

Figure 3

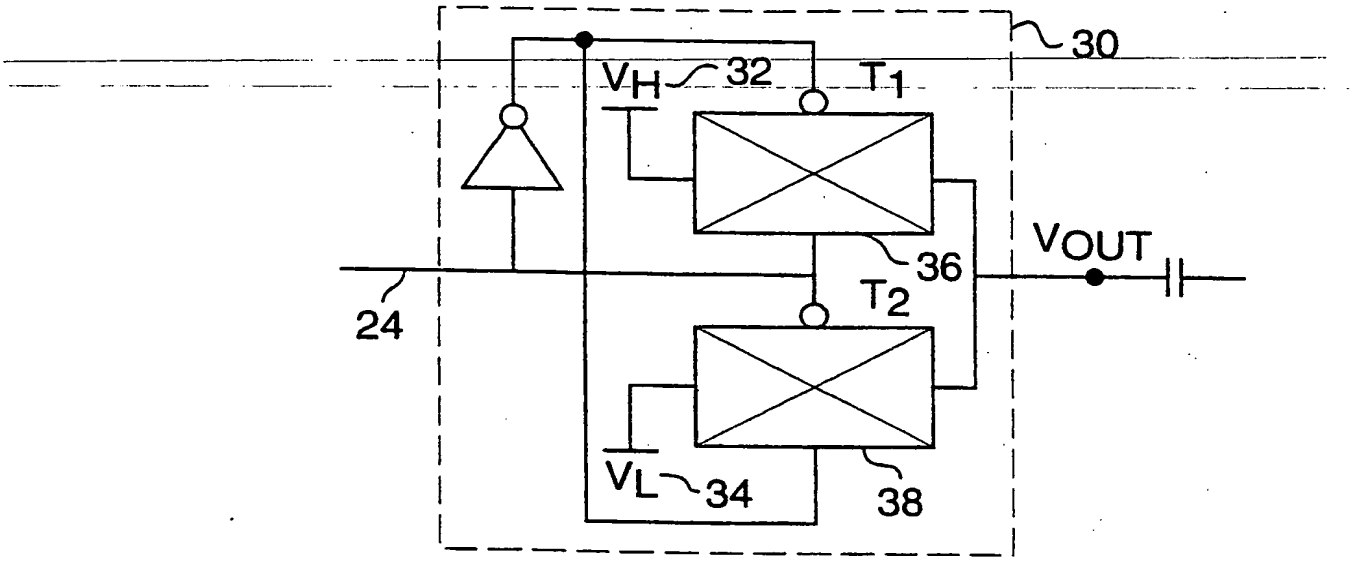

Figure 4

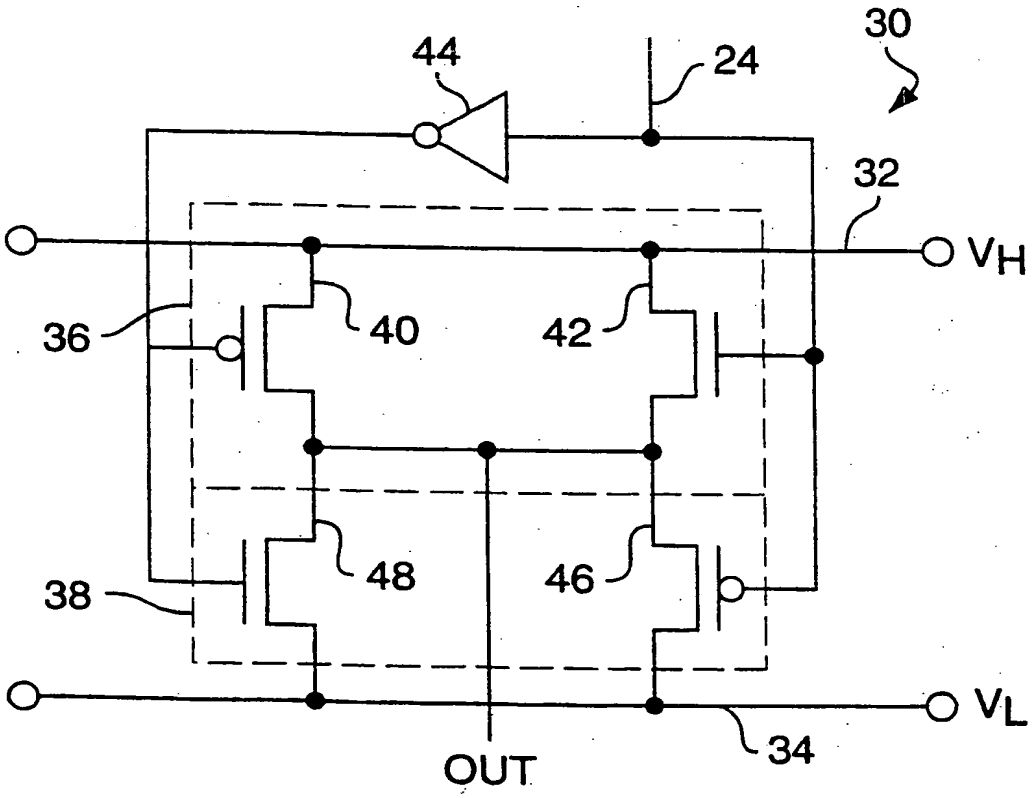

Figure 5

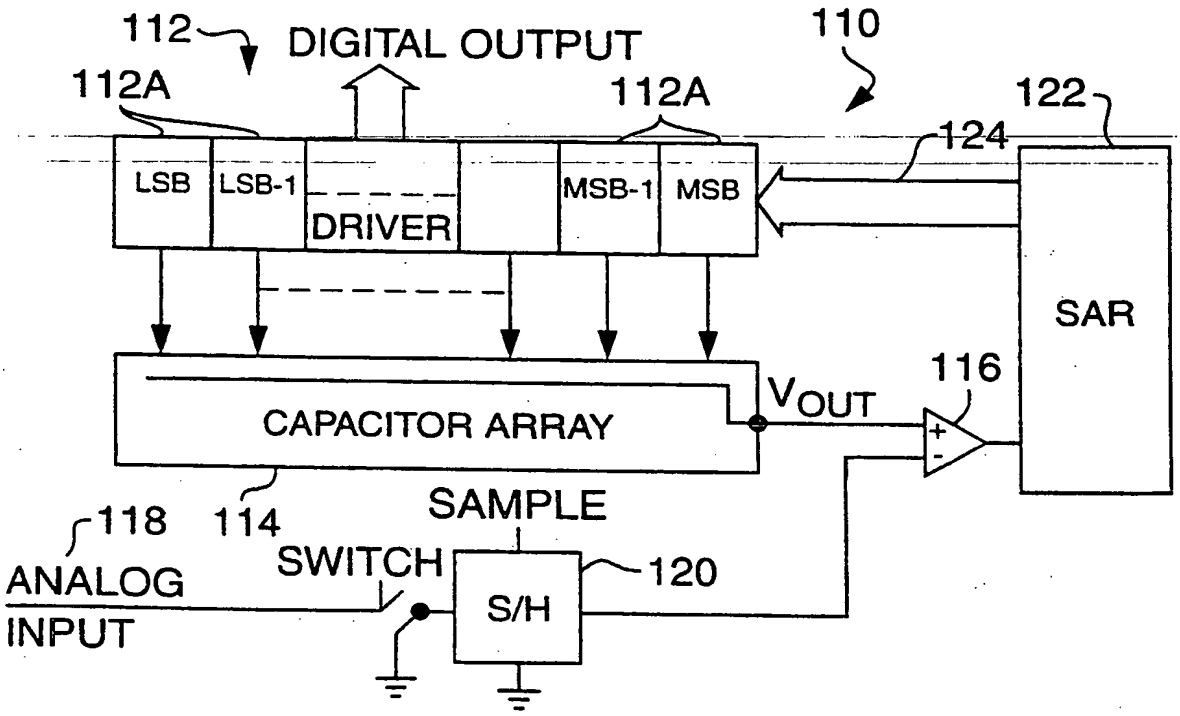

Figure 6

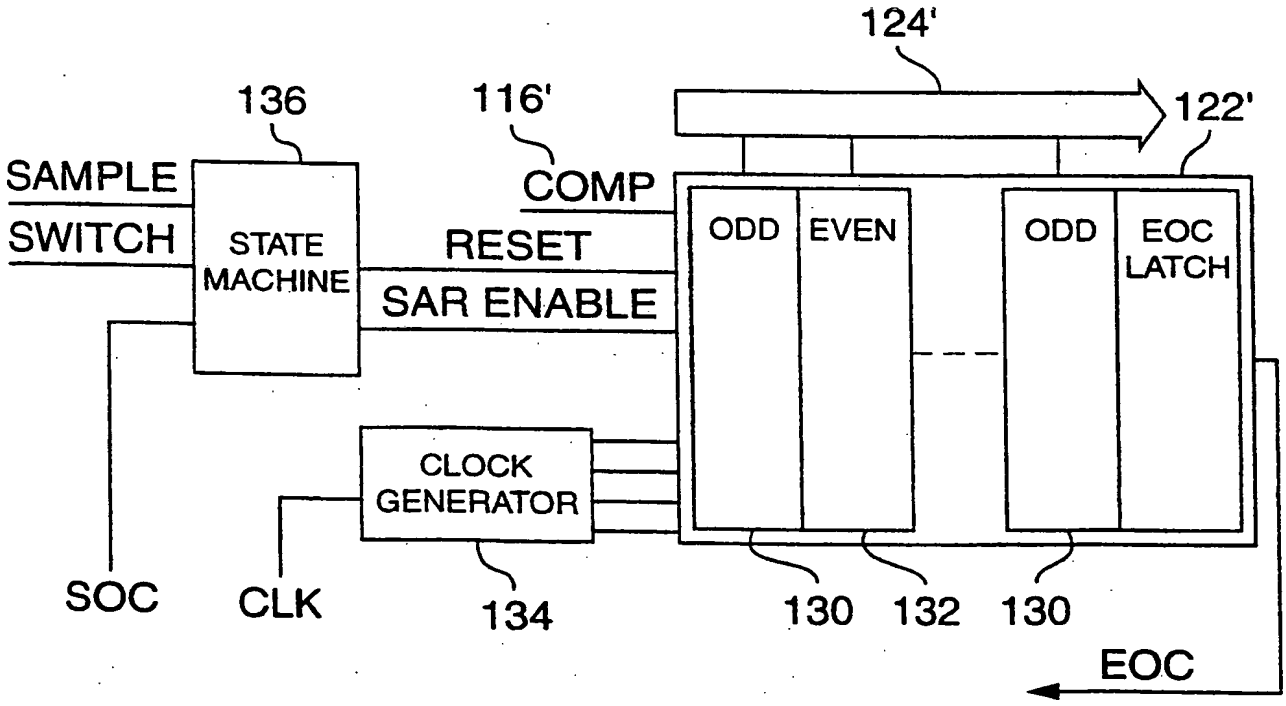

Figure 7

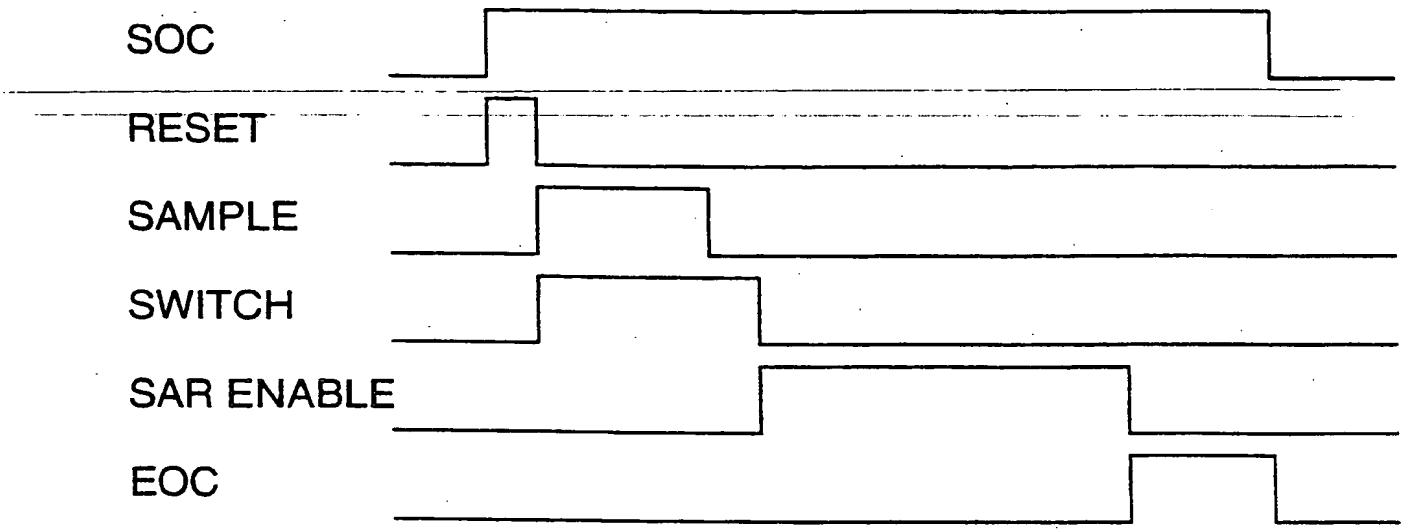

Figure 8

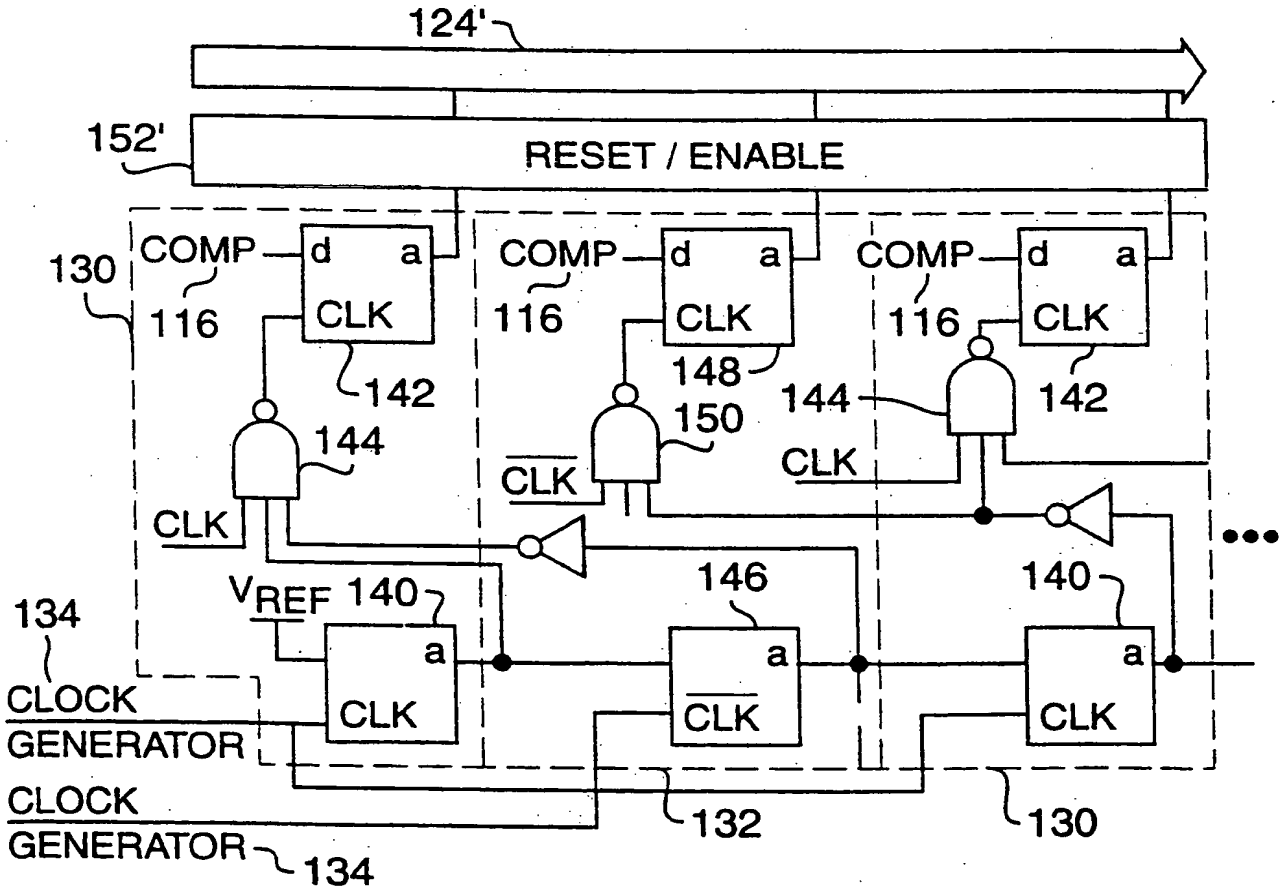

Figure 9

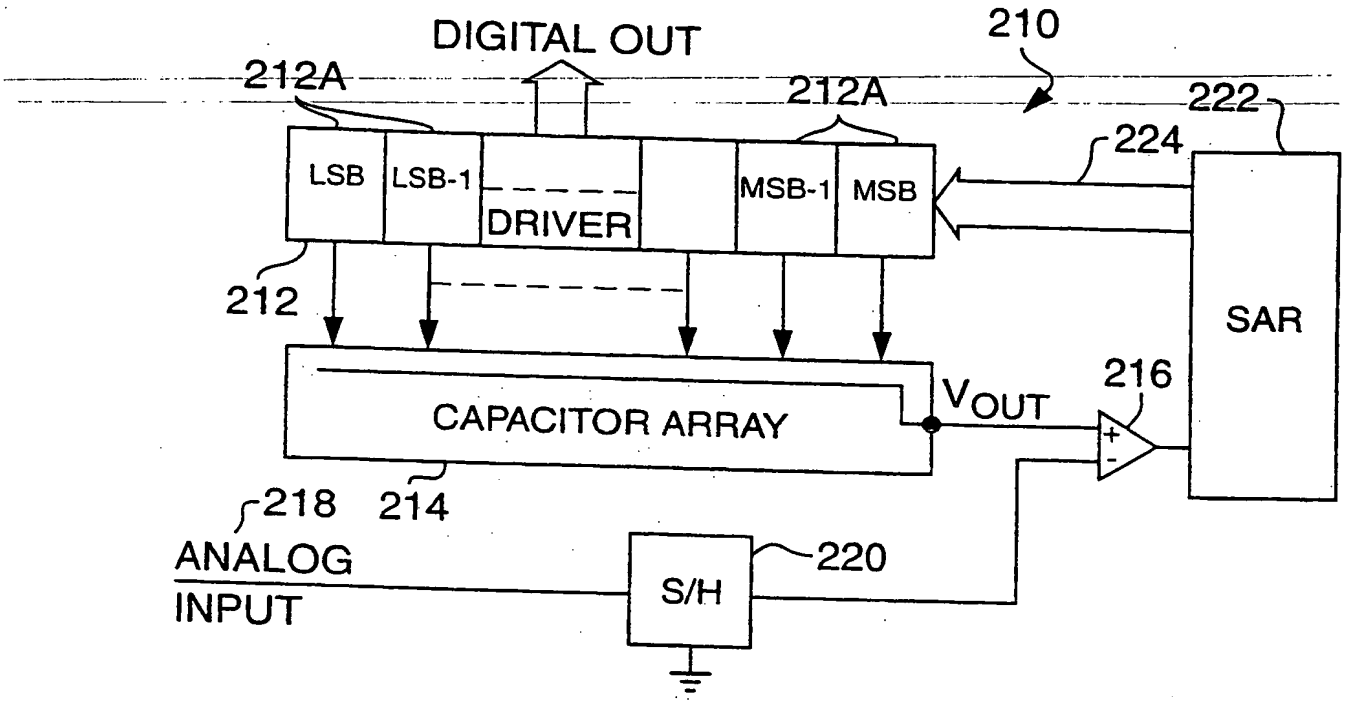

Figure 10

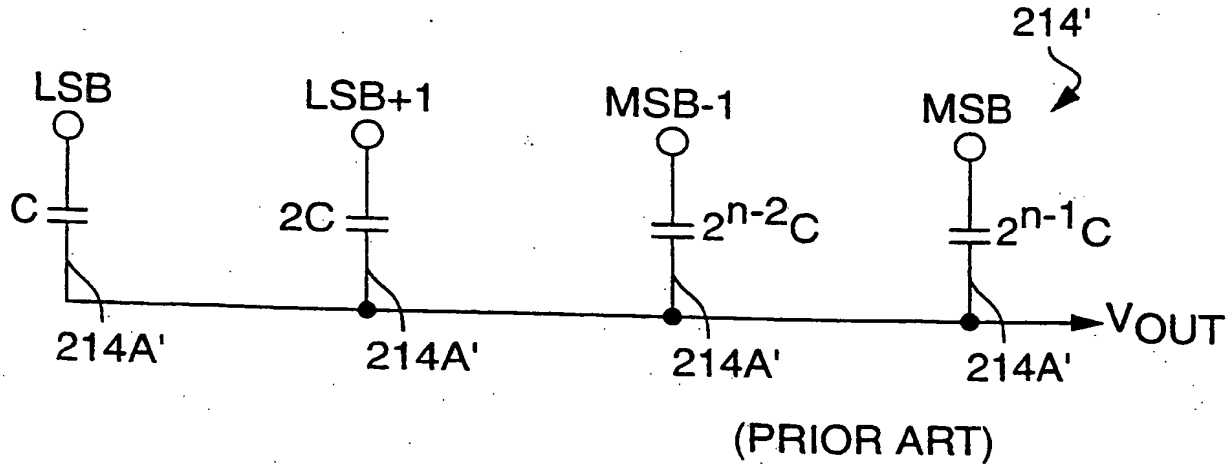

Figure 11

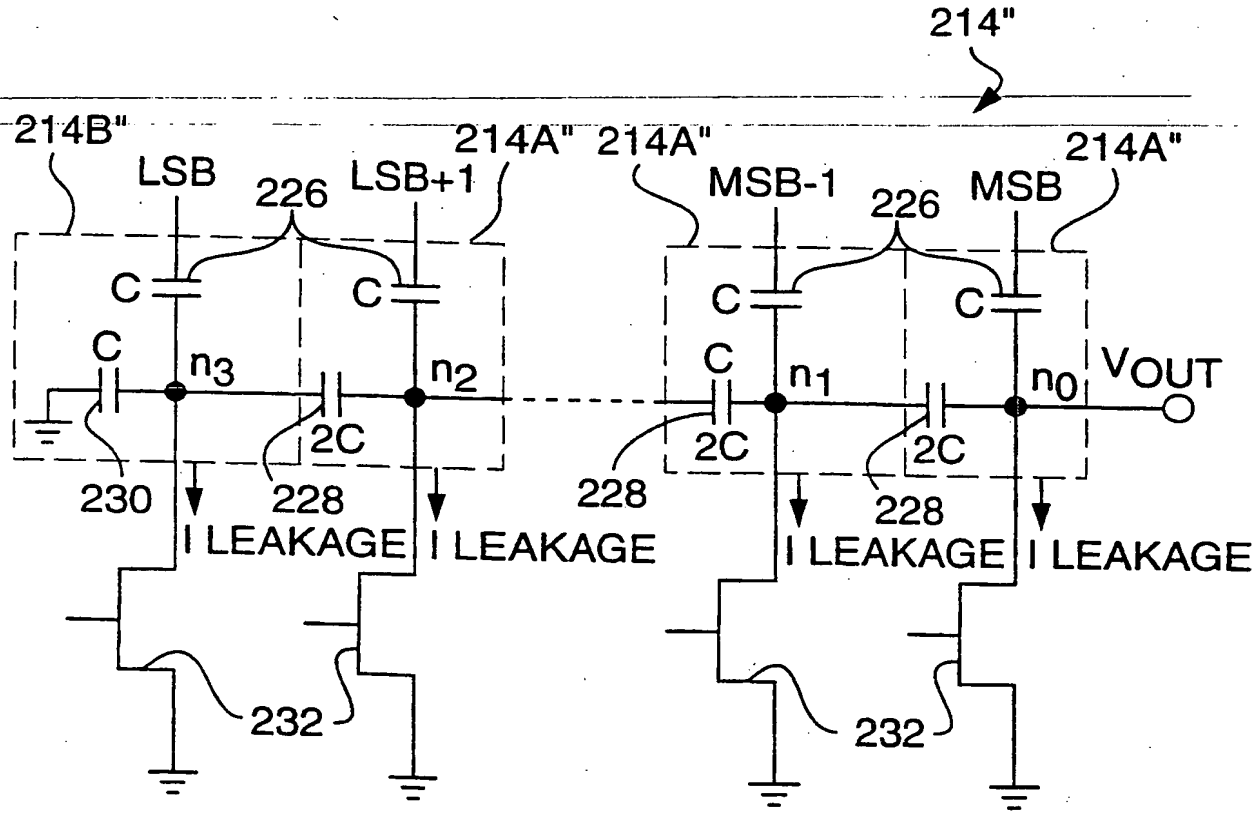

Figure 12

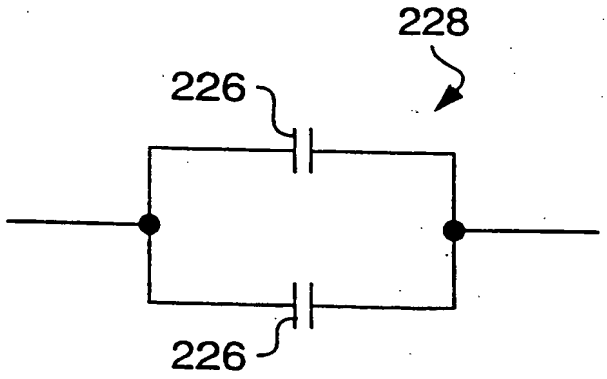

Figure 13

INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/US 99/01186

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03M1/46 H03M1/78 H03M1/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 611 195 A (SHOSAKU TSUKAGOSHI) 9 September 1986 see column 5, line 32 - line 36; figure 5	1-16
X	GB 2 096 848 A (WESTERN ELECTRIC CO) 20 October 1982 see page 5, line 31 - line 48; figure 6	1-16
A	US 4 641 130 A (MASTROIANNI ANTHONY R) 3 February 1987 see figure 2	1-16

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 April 1999	04/05/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Verhoof, P

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INTERNATIONAL SEARCH REPORT

information on patent family members

Interr ...al Application No
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